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Term: 12 and 17

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Wednesday, March 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L11	l2 and l7	1	L11
L10	l7 same (I/O or peripheral)	16	L10
L9	l7 and PCMCIA	2	L9
L8	external device same l7	1	L8
L7	(address adj2 (translation or translating or translation or translator)) same ((bus adj2 width) or control information or attribute or memory accessing or access timing) same (map or table or directory)	205	L7
L6	l4 and PCMCIA	1	L6
L5	l2 and l4	0	L5
L4	(address adj2 (translation or translating or translation or translator)) same ((bus adj2 width) or control information)	245	L4
L3	(address adj2 (translation or translating or translation)) same ((bus adj2 width) or control information)	231	L3
L2	((dynamic or dynamically or program or programmable or change or changing) adj4 (bus adj3 width)) same (controller or control unit or microcomputer or microprocessor or processor or CPU)	74	L2

L1	(dynamic or dynamically or program or programmable or change or changing) same (bus adj3 width) same PCMCIA same (controller or control unit or microcomputer or microprocessor or processor or CPU)	7	L1

END OF SEARCH HISTORY

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9
Best 200 shown

1 Design methodology of a 200MHz superscalar microprocessor: SH-4
Toshihiro Hattori, Yusuke Nitta, Mitsuho Seki, Susumu Narita, Kunio Uchiyama, T
May 1998 Proceedings of the 35th annual conference on Design automation co
Full text available: pdf(282.85 KB) Additional Information: full citation, abstract, references,

A new design methodology focusing on high speed operation and short design superscalar microprocessor. Random test generation, logic emulation, and forr verification for shortening design time. Delay budgeting, forward/back annotat for timing driven design.

Keywords: design methodology, microprocessor, timing, verification

2 Going the distance for TLB prefetching: an application-driven study
Gokul B. Kandiraju, Anand Sivasubramaniam
May 2002 ACM SIGARCH Computer Architecture News , Proceedings of the 29th a Computer architecture, Volume 30 Issue 2
Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, refere

The importance of the Translation Lookaside Buffer (TLB) on system performar numerous prior efforts addressing TLB design issues for cutting down access ti it was only recently that the first exploration [26] on prefetching TLB entries al mechanism called Recency Prefetching was proposed. There is a large body of it is not clear how they can be ada ...

Keywords: application-driven study, memory hierarchy, prefetching, simulatior

Google

Advanced Search Preferences Language Tools Search Tips

TLB and PCMCIA

Google Search

The **"AND"** operator is unnecessary -- we include all search terms by default. [details]

Web Images Groups Directory News

Searched the web for **TLB and PCMCIA**. Results **31 - 40** of about **5,900**. Search took **0.16** seconds.

[PDF]Windows CE System solution by Toshiba Windows CE Windows CE ...
File Format: PDF/Adobe Acrobat - View as HTML
... LCD Interface Power management Timer 2 Ch SIO Memory Controller CPU Core I$ 4KB
D$ 1KB **TLB** TX39 Core IRC PIO **PCMCIA** I/F RTC TX3912 - Block Diagram TX3912 ...
www2.abacus.co.uk/microsoft/toshce.pdf - Similar pages

PowerQUICC MPC860 FAQ
The summary for this Japanese page contains characters that cannot be correctly displayed in this language/character set.
www.mot.co.jp/SPS/html/faq/mpc860-1-2.html - 63k - Cached - Similar pages

[PDF]MPC860TS: MPC860 PowerQUICC Technical Summary
File Format: PDF/Adobe Acrobat - View as HTML
... A **PCMCIA** socket controller supports up to two sockets ... recently used (LRU) replacement,
lockable on-line granularity - MMUs with 32 entry **TLB**, fully associative ...
www.mot.co.jp/SPS/html/lit/pdf/mpc860ts_r0.1.pdf - Similar pages
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Linux-Kernel Archive: Re: [x86-64] Add missing **tlb** flush after
... Next message: Dominik Brodowski: "[CFT/RFC] **pcmcia** bus driver as an interface to ... In
reply to: davej@codemonkey.org.uk: "[x86-64] Add missing **tlb** flush after ...
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File Format: PDF/Adobe Acrobat
... TX39 / H Processor Core + **TLB** Memory Controller **PCMCIA** Controller Communications
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www.sumisho.co.kr/product/semiconductor/ pdf/4400c_03.pdf - Similar pages

Windows CE and PocketPC Palmtop Computers
... 40 MHz MIPS 3910 CPU core in a Philips PR35100, providing 1 KB data cache and 4 KB instruction cache, **TLB**, timers and real time clock, **PCMCIA** interface, memory ...

Your search matched **1** of **947413** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
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Then click **Search Again**.

pcmcia and tlb

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operation unit**
Nishii, O.; Arakawa, F.; Ishibashi, K.; Nakano, S.; Shimura, T.; Suzuki, K.; Tachibana, M.; Totsuka, Y.; Tsunoda, T.; Uchiyama, K.; Yamada, T.; Hattori, T.; Maejima, H.; Nakagawa, N.; Narita, S.; Seki, M.; Shimazaki, Y.; Satomura, R.; Takasuga, T.; Hasega
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International , 5-7 Feb. 1998
Page(s): 288 -289, 447

[Abstract] [PDF Full-Text (1216 KB)] **IEEE CNF**

WEST

End of Result Set

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L3: Entry 4 of 4 File: JPAB Sep 2, 1998

PUB-NO: JP410232850A
DOCUMENT-IDENTIFIER: JP 10232850 A
TITLE: EXTENSION CARD DEVICE AND EXTENSION CARD CONTROL METHOD

PUBN-DATE: September 2, 1998

INVENTOR-INFORMATION:
NAME COUNTRY
NOBUTANI, TOSHIYUKI

ASSIGNEE-INFORMATION:
NAME COUNTRY
CANON INC

APPL-NO: JP09035763
APPL-DATE: February 20, 1997

INT-CL (IPC): G06 F 13/36

ABSTRACT:

PROBLEM TO BE SOLVED: To reduce radiation noises with data transfer while improving data transfer throughput by limiting unwanted data transfer access by outputting data, which are to be outputted to an internal bus, onto an external bus when a detecting means detects data transfer access to the external bus.

SOLUTION: An address recorder 201 analyzes an address to be outputted to an internal bus PCMCIA and detects the data transfer access to an external bus EB. When the address recorder 201 detects the data transfer access to the external bus EB, an address translation circuit 202 controls data transfer so as to output the data, which are to be outputted to the internal bus PCMCIA, onto the external bus EB. Thus, when extending the internal bus PCMCIA to the external bus EB, data transfer is enabled by detecting access to the external bus EB and the radiation noises with data transfer can be reduced while improving data transfer throughput while limiting the unwanted data transfer access.

WEST

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L4: Entry 27 of 44 File: USPT Jun 12, 2001

DOCUMENT-IDENTIFIER: US 6247084 B1
TITLE: Integrated circuit with unified memory system and dual bus architecture

Detailed Description Text (17):
Integrated circuit 10 further includes processor 12, memory controller 14, bus transactor circuits 15A-15C, data bus 22 and command bus 24. In one embodiment, processor 12 includes a CW4011 Microprocessor Core available from LSI Logic Corporation, a Multiply/Shift Unit, a MMU/TLB, 16K instruction cache, 8K data cache, and a Cache Controller/Bus Interface Unit. The CW4011 core is a MIPS.RTM. architecture processor that implements the R4000, MIPS.RTM. II compliant 32--bit instruction set. Other types of processors can also be used.

Detailed Description Text (21):
Subsystem 126A is a serial I/O subsystem which implements a fast Ethernet 10 Mbit/100 Mbit per second peripheral device, a four port universal serial bus host controller, an audio-97 AC-link audio peripheral and a set of generic programmed I/O pins. Subsystem 126B is a PCI and parallel I/O subsystem which includes a high performance PCI interface, an IEEE 1284 compliant parallel port, and IDE/ATA-PI disk interface, provisions for flash ROM and PCMCIA adapters, PS2 compatible keyboard and mouse inputs, I.sup.2 C interfaces and a SmartCard interface.

Detailed Description Text (186):
FIG. 17 is a block diagram of processor 12 according to one embodiment of the present invention. Processor 12 includes a CW4011 Microprocessor Core 250, which is available from LSI Logic Corporation, a multiply/accumulate Unit 252, a memory management unit (MMU) 254 with a translation lookaside buffer (TLB), a 16K two-way set associative instruction cache 256, an 8K two-way set associative data cache 258, a write-back buffer 260 for write cache mode and an SCbus interface 262. The CW4011 core is a MIPS.RTM. architecture processor that implements the R4000, MIPS.RTM. II compliant 32-bit instruction set. Other types of processors can also be used.

Detailed Description Text (484):
Subsystem 126B preferably has the following features: a Dual Port RAM interface to system buses 22 and 24, a High performance PCI interface; an IEEE 1284 Parallel Port; IDE/ATA-PI Disk interface; Provisions for Flash ROM and PCMCIA adapters; PS2 compatible keyboard and mouse inputs; I2C interfaces; and a Smart Card interface.

Detailed Description Text (487):
ATA-PI/Flash ROM/PCMCIA preferably have the following functions: Direct support of IDE/ATA-PI compatible disk drives; Provisions for addressing Flash ROM (executable); Provisions for interfacing to PCMCIA bridges; ATA-2 standard (ANSI X3.279-1996); PCMCIA PC Card Standard Release 2.1.

Detailed Description Text (489):
Detailed descriptions of the parallel interfaces can be found in the following documents: IEEE Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers (ANSI); PCI Local Bus Specification, revision 2.1; ATA-2 standard (ANSI X3.279-1996); and PCMCIA PC Card Standard Release 2.1.

L4: Entry 10 of 44 File: USPT May 13, 2003

DOCUMENT-IDENTIFIER: US 6564329 B1
TITLE: System and method for dynamic clock generation

Detailed Description Text (4):
The DSP 114 provides a digital signal processing engine for applications such as speech recognition, data compression, modem and other forms of communication, and other real time applications where complex signal processing is desired. In one embodiment, the cache 118 is an 8 Kilobyte (KB) unified cache with a 64-entry translation lookaside buffer (TLB). Preferably, the DSP 114 and cache 118 are integrated into the CPU 112 core in order to enhance the performance of the CPU.

Detailed Description Text (8):
In addition, the portable electronic device 100 may have one or more interfaces for accepting function cards 136. These cards include smart cards, MMC cards, Personal Computer Memory Card International Association (PCMCIA) cards, and flash memory cards providing functionality such as additional memory storage, audio codecs, software, display interfaces, electronic commerce transactions, and any other functionality that can be included on a card.

Detailed Description Text (10):
FIG. 2 is a block diagram illustrating the internal functional units of the ASIC 110 according to one embodiment of the present invention. The CPU 112 contains the cache 118 and is coupled to the DSP 114 and a system bus 210. The system bus 210 couples a memory controller 212, an on-chip static random access memory (SRAM) 214, an interrupt controller 216, a peripheral bridge 218 and a PCMCIA interface 220.

Detailed Description Text (16):
The system bus 210 is also coupled to a static memory interface 220. The static memory interface 220 can interface with devices like read only memory (ROM), SRAM, flash memory, and PCMCIA 2.0 compliant devices.

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L1: Entry 7 of 7 File: USPT Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5778195 A
TITLE: PC card

Detailed Description Text (23):
The PC card has the communication function and the memory function, and it performs the three modes of operation similar to those of the PC card of the first embodiment. In a situation where the PC card is used as a memory card, when the PC card is inserted in a system equipment, the system equipment transmits a request of communication to the PC card. Then, the PCMCIA interface controller 101 of the PC card changes the configuration to a communication card. Detailed explanation is omitted here because the operation is the same as that in the first embodiment. In a situation where the PC card is used as a memory card, when the PC card is inserted in a system equipment such as a personal computer, the system equipment transmits a request of memory access to the PC card. Then, the PCMCIA interface controller 101 of the PC card changes the configuration to a memory card and activates the memory controller 103. Next, according to instructions from the system equipment, the PCMCIA interface controller 101 sets an address signal at the address bus 112a, a data signal at the data bus 113a, and activates the output enable bus 116. Then, the data signal is output from the memory device 104 to the data bus 113b. Further, when a data signal is set at the data bus 113b, and the write enable bus 117 is activated, the data is written to the memory 104. Because the bus width for the memory function is wider, the memory device 104 can be accessed at a faster speed.

First Hit Fwd Refs

End of Result Set

☐ Generate Collection Print

L11: Entry 1 of 1 File: USPT Aug 8, 1995

DOCUMENT-IDENTIFIER: US 5440708 A
TITLE: Microprocessor and storage management system having said microprocessor

Detailed Description Text (4):
FIG. 1 shows the outline of storage management to which the present invention is adapted, and wherein reference numeral 100 denotes a logical space (virtual storage) that serves as a virtual storage space and that is expressed by logical addresses (virtual addresses) on the architecture, 4 denotes a physical space (real storage) that exists as hardware and that is referred to by physical addresses (real addresses), 5 denotes a peripheral storage such as a magnetic disc device, and symbol AT denotes a logical space management table which shows a relationship between logical addresses on the logical space and physical addresses on the physical space and which, at the time of address translation, makes reference to the contents in the logical space management table AT and translates logical address into physical address. In this storage management, the physical space 4 to which access is made with physical address is referred to as primary memory and the peripheral storage 5 is referred to as secondary memory. Though there is no particular limitation, the logical space 100 is corresponding to a page of the secondary memory 5. When the page on the logical space 100 does not exist on the primary memory 4, the page on the secondary memory 5 is taken in onto the primary memory 4 by the interposition of, for example, the operating system. In this case, when there is no vacancy in the primary memory 4, some pages are saved in the secondary memory 5 and new pages are inserted therein. Reference data and change data of physical page are utilized to replace the pages. The reference data are those which indicate whether reference is made to the stored data on the physical space 4, and the change data are those which indicate whether the stored data are rewritten or not on the primary memory 4. At the time of replacing the pages, if there is a page which is neither referred to nor changed, the contents thereof are not saved but are expelled out of the physical space 4. When a page that is changed is to be expelled, on the other hand, the contents thereof are saved. The reference/change data of physical page are used as attribute data related to the physical space 4 together with bus size data that will be described later. The attribute data are held by a physical space management table PMT corresponding to physical addresses. The physical space management table PMT is constituted on the physical space 4 independently of the logical space management table AT and updates predetermined attribute data depending upon the conditions of writing onto corresponding physical addresses.

Detailed Description Text (44):
In this embodiment, the pipeline operation of the bus is carried out even at a change of the bus size. This is because, the bus control unit BIF provided in the microprocessor 1 receives the bus size data output from the physical data buffer PIB in response to a physical address that is output, and forms a signal for byte control and outputs it. In the case of the conventional dynamic bus sizing, the bus width for the address a is reported from the external bus controller at a moment of clock 2 or 3. Therefore, the microprocessor effects the addition operation of addresses therein at the clock 3 at the earliest, and does not issue the next address after the clock 3. As described above, the bus size data of physical

address are designated in advance via the physical space management table, enabling the address pipeline and the bus sizing to be compatible with each other.

Detailed Description Text (53):
FIG. 12(b) shows the condition of the change bit M up to the lapse of time 6 when the change bit M exists on the address translation table. In this case, the data written onto the virtual page are managed. As for the processor 1-1, therefore, the virtual page 1 and the virtual page 5 having the same content a assigned to the physical page 1 have change bits M which are different from each other. That is, as schematically shown in FIG. 1, this is the condition where the logical pages 1, 5 of logical space 100 are assigned with the lapse of time to the physical page 1 of the physical space 4, and the changed bits M are held in separate places of the logical space management table AT corresponding to the logical pages 1 and 5. Moreover, the logical page 3 has the same content c but has different change bits M for the processors 1-1 and 1-2. This is because, the microprocessors 1-1 and 1-2 manage the attribute data such as change bit M in a manner corresponding to the logical space via their own logical space management systems 2-1 and 2-2. Therefore, the operating system must carry out the logical space management upon fully recognizing this fact; i.e., processing becomes complex such as replacement of pages and extended periods of time are needed for the processing.

L10: Entry 8 of 16 File: USPT Jun 9, 1981

DOCUMENT-IDENTIFIER: US 4272819 A
** See image for Certificate of Correction **
TITLE: Inter-subsystem direct transfer system

Detailed Description Text (4):
FIG. 3 is explanatory of the formation of the enqueue command and the queue elements SSCB. It shows a priority indicating register 7A; a program status control word 12A; a control register 0 13A; a control register 1 14A; a memory fixed space 15A; a program status word PSW key KEY; a bit P indicating whether the mode of operation is a problem or supervisor mode; a segment size SS; a page size PS; a segment table address STA; a segment table length STL; the content PRLR of the priority indicating register 7A; a program identify for identifying a program having issued an enqueue command; and TEXT the content of a request or answerback. The enqueue command has first and second operands. The first operand (B.sub.1, D.sub.1) assigns the text and the second operand (B.sub.2, D.sub.2) assigns the subsystem address, the text length and the inform priority of the destination subsystem. The queue element SSCB has, as parameters, the queue element length, the inform priority, the PSW key and P-bit, the segment size SS and the page size PS, the segment table address STA and the segment table length STL, the priority value of the priority indicating register, and the program identify of a program having issued the enqueue command and the text. As the PSW key, bits 8 to 11 of the program status word are inserted. The PSW key is used for storage protection when the memory 3A (or 3B) is accessed. As the page size PS, bits 8 to 9 of the control register 0 13A are inserted. As the segment table length STL, bits 0 to 7 of the control register 1 14A are inserted and, as the segment table address STA, bits 8 to 25 of the control register 1 14A are inserted. The page size PS, the segment size SS, the segment table length STL and the segment table address STA are included in the queue element SSCB issued from the host subsystem A and used as DAT (Dynamic Address Translation) control information when the I/O sybsystem B accesses the memory 3A of the host subsystem A using a virtual address.

Detailed Description Text (5):
When the I/O subsystem B directly accesses the memory 3A of the host subsystem A, the former is supplied with host memory access control information by such means as mentioned above. Accordingly, when convenient, the I/O subsystem B can directly access the memory 3A of the host subsystem A without intervention of the processor of the host subsystem A. Next, a description will be given of the EXMVL instruction for executing direct access and a method of direct access. FIG. 4 is explanatory of the EXMVL instruction. The EXMVL instruction has a first operand part R.sub.1, a second operand part B.sub.2, D.sub.2 and a third operand part R.sub.3. The first operand part R.sub.1 is to assign a register having stored therein a destination head address and a destination byte count, and the third operand R.sub.3 is to assign a register having stored therein a source head address and a source byte count. In the address area assigned by the second operand B.sub.2, D.sub.2, there have been stored the other subsystem address SA, transfer direction assign information D, mode assign information R indicating whether or not the dynamic address transfer is carried out, a PSW key, a segment table address STA, a page size PS and a segment size SS. The transfer direction assign information D of logic "0" indicates that data should be transferred from the other subsystem. The transfer direction assign information D of logic "1" indicates that data should be

transferred to the other subsystem. The mode assign information R of logic "0" indicates the execution of a dynamic address translation, that is, a virtual mode. The mode assign information R of logic "1" indicates non-execution of the dynamic address translation, that is, a real mode. The PSW key, the segment table length STL, the segment table address STA, the page size PS and the segment size SS make up memory access control information. The memory access control information stored in the address area assigned by the second operand B.sub.2, D.sub.2 of the EXMVL instruction is identical with the memory access information included in the queue element on which is based the issuance of the EXMVL instruction. Reference character PAD indicates a padding character.

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